What is claimed is:

1. A method for creation of stacked layers of polysilicon, comprising:

providing a substrate, at least one pattered first layer of polysilicon having been created over said substrate;

depositing a second layer of polysilicon over said substrate, thereby including the at least one pattered first layer of polysilicon; and

etching said second layer of polysilicon, thereby removing remnants of the second layer of polysilicon from sidewalls of the at least one pattered first layer of polysilicon.

2. The method of claim 1, said etching said second layer of polysilicon comprising BT-ME-OE-flash.

3. The method of claim 2, said BT comprising a pressure of between about 3 and 5 mTorr, source power between about 200 and 300 Watt, bias power between about 100 and 200 Watt, etchant gas Cl_2 supplied at between about 80 and 100 sccm, applied for a time of between about 8 and 12 seconds.

4. The method of claim 2, said ME comprising a pressure of between about 5 and 7 mTorr, source power between about 200 and 300 Watt, bias power between about 100 and 200 Watt, etchant gas

Cl_2 supplied at between about 25 and 35 sccm with HBr supplied at between about 80 and 100 sccm with an OE of about 15%.

5. The method of claim 2, said OE comprising a pressure of between about 50 and 70 mTorr, source power between about 200 and 300 Watt, bias power between about 150 and 220 Watt, etchant gas HBr supplied at between about 150 and 250 sccm with He supplied at about 80 to 120 sccm, with $He-O_2$ supplied at between about 3.0 and 3.0 sccm.

6. The method of claim 2, said flash step comprising a pressure of between about 50 and 70 mTorr, source power between about 100 and 200 Watt, etchant gas SF_6 supplied at between about 40 and 60 sccm with He supplied at about 150 to 250 sccm, applied for between about 10 and 20 sec.

7. A method for the stacked layers of gate material for creation of mixed-mode semiconductor devices, comprising:

providing a substrate;

creating a layer of gate oxide over said substrate;

depositing a first layer of gate material over said layer of gate oxide;

patterning and first etching said layer of first gate material;

depositing a layer of inter-polysilicon dielectric material over said substrate, thereby including exposed surfaces of said first etched layer of first gate material;

depositing a second layer of gate material over said layer of inter-polysilicon dielectric material; and

patterning and second etching said second layer of gate material.

8. The method of claim 7, said first layer of gate material comprising polysilicon.

9. The method of claim 7, said second layer of gate material comprising polysilicon.

10. The method of claim 7, said inter-polysilicon dielectric material comprising oxide based material.

11. The method of claim 7, said patterning and second etching said second layer of gate material comprising steps BT-ME-OE-flash step.

12. The method of claim 11, said BT comprising a pressure of between about 3 and 5 mTorr, source power between about 200 and 300 Watt, bias power between about 100 and 200 Watt, etchant gas

Cl_2 supplied at between about 80 and 100 sccm, applied for a time of between about 8 and 12 seconds.

13. The method of claim 11, said ME comprising a pressure of between about 5 and 7 mTorr, source power between about 200 and 300 Watt, bias power between about 100 and 200 Watt, etchant gas Cl_2 supplied at between about 25 and 35 sccm with HBr supplied at between about 80 and 100 sccm with an OE of about 15%.

14. The method of claim 11, said OE comprising a pressure of between about 50 and 70 mTorr, source power between about 200 and 300 Watt, bias power between about 150 and 220 Watt, etchant gas HBr supplied at between about 150 and 250 sccm with He supplied at about 80 to 120 sccm, with He-O_2 supplied at between about 3.0 and 3.0 sccm.

15. The method of claim 11, said flash step comprising a pressure of between about 50 and 70 mTorr, source power between about 100 and 200 Watt, etchant gas SF_6 supplied at between about 40 and 6 sccm with He supplied at about 150 to 250 sccm, applied for between about 10 and 20 sec.

16. A method for creation of stacked layers of polysilicon, comprising:

providing a substrate, at least one pattered first layer of polysilicon having been created over said substrate;

depositing a second layer of polysilicon over said substrate, thereby including the at least one pattered first layer of polysilicon; and

etching said second layer of polysilicon, thereby removing remnants of the second layer of polysilicon from sidewalls of the at least one pattered first layer of polysilicon, said etching said second layer of polysilicon comprising BT-ME-OE-flash.

17. The method of claim 16, said BT comprising a pressure of between about 3 and 5 mTorr, source power between about 200 and 300 Watt, bias power between about 100 and 200 Watt, etchant gas Cl_2 supplied at between about 80 and 100 sccm, applied for a time of between about 8 and 12 seconds.

18. The method of claim 16, said ME comprising a pressure of between about 5 and 7 mTorr, source power between about 200 and 300 Watt, bias power between about 100 and 200 Watt, etchant gas Cl_2 supplied at between about 25 and 35 sccm with HBr supplied at between about 80 and 100 sccm with an OE of about 15%.

19. The method of claim 16, said OE comprising a pressure of between about 50 and 70 mTorr, source power between about 200 and

300 Watt, bias power between about 150 and 220 Watt, etchant gas HBr supplied at between about 150 and 250 sccm with He supplied at about 80 to 120 sccm, with He-O_2 supplied at between about 3.0 and 3.0 sccm.

20. The method of claim 16, said flash step comprising a pressure of between about 50 and 70 mTorr, source power between about 100 and 200 Watt, etchant gas SF_6 supplied at between about 40 and 60 sccm with He supplied at about 150 to 250 sccm, applied for between about 10 and 20 sec.

21. A method for the stacked layers of polysilicon for creation of mixed-mode semiconductor devices, comprising:

providing a substrate;

creating a layer of gate oxide over the surface of said substrate;

depositing a first layer of gate material over said layer of gate oxide;

patterning and first etching said layer of first gate material;

depositing a layer of inter-polysilicon dielectric material over the surface of said substrate, thereby including exposed surfaces of said first etched layer of first gate material;

depositing a second layer of gate material over the surface of said layer of inter-polysilicon dielectric material; and

patterning and second etching said second layer of gate material, said patterning and second etching said second layer of gate material comprising steps BT-ME-OE-flash step.

22. The method of claim 21, said first layer of gate material comprising polysilicon.

23. The method of claim 21, said second layer of gate material comprising polysilicon.

24. The method of claim 21, said inter-polysilicon dielectric material comprising oxide based material.

25. The method of claim 21, said BT comprising a pressure of between about 3 and 5 mTorr, source power between about 200 and 300 Watt, bias power between about 100 and 200 Watt, etchant gas Cl_2 supplied at between about 80 and 100 sccm, applied for a time of between about 8 and 12 seconds.

26. The method of claim 21, said ME comprising a pressure of between about 5 and 7 mTorr, source power between about 200 and 300 Watt, bias power between about 100 and 200 Watt, etchant gas

Cl_2 supplied at between about 25 and 35 sccm with HBr supplied at between about 80 and 100 sccm with an OE of about 15%.

27. The method of claim 21, said OE comprising a pressure of between about 50 and 70 mTorr, source power between about 200 and 300 Watt, bias power between about 150 and 220 Watt, etchant gas HBr supplied at between about 150 and 250 sccm with He supplied at about 80 to 120 sccm, with $He-O_2$ supplied at between about 3.0 and 3.0 sccm.

28. The method of claim 21, said flash step comprising a pressure of between about 50 and 70 mTorr, source power between about 100 and 200 Watt, etchant gas SF_6 supplied at between about 40 and 6 sccm with He supplied at about 150 to 250 sccm, applied for between about 10 and 20 sec.

29. A stack of layers of polysilicon, comprising:

a substrate, at least one pattered first layer of polysilicon having been created over said substrate;

a second layer of polysilicon having been deposited over said substrate, thereby including the at least one pattered first layer of polysilicon; and

said second layer of polysilicon having been patterned, thereby removing remnants of the second layer of polysilicon from

sidewalls of the at least one pattered first layer of polysilicon.

30. A stack of layers of gate material for creation of mixed-mode semiconductor devices, comprising:

a substrate;

a layer of gate oxide created over said substrate;

a patterned first layer of gate material deposited over said layer of gate oxide;

a layer of inter-polysilicon dielectric material deposited over said substrate, thereby including exposed surfaces of said patterned first layer of gate material;

a patterned second layer of gate material deposited over said layer of inter-polysilicon dielectric material, having thereby removed remnants of the patterned second layer of polysilicon from sidewalls of the patterned first layer of polysilicon.

31. The stacked of layers of gate material of claim 30, said first layer of gate material comprising polysilicon.

32. The stacked of layers of gate material of claim 30, said second layer of gate material comprising polysilicon.

33. The stacked of layers of gate material of claim 30, said inter-polysilicon dielectric material comprising oxide based material.